CLAIMS

What is claimed is:

1. A method, comprising:

sensing a saturation of a common mode feedback amplifier in a fully differential amplifier; and

returning the fully differential amplifier to a normal mode of operation based on the sensing of the saturation of the common mode feedback amplifier.

2. The method of claim 1, wherein sensing comprises receiving a common mode feedback signal at an input of a sense circuit and wherein the method further comprises receiving a supply voltage signal on inputs and outputs of the fully differential amplifier.

3. The method of claim 2, wherein returning comprises lowering the outputs of the fully differential amplifier.

4. The method of claim 3, wherein returning further comprises pushing up voltages of internal nodes of the fully differential amplifier, the internal nodes coupled to gates of the output transistors of the fully differential amplifier.

5. The method of claim 4, wherein returning further comprises turning on the output transistors of the fully differential amplifier to lower the outputs of the fully differential amplifier.

6. The method of claim 1, wherein the fully differential amplifier further comprises input transistors, and wherein the sensing of the saturation is performed when the input transistors are in a cut-off state.

7. A fully differential amplifier, comprising:

a first stage comprising a common mode feedback amplifier;

a second stage comprising a plurality of input transistors; and

a start-up circuit coupled between the first and second stages.

8. The fully differential amplifier of claim 7, wherein the start-up circuit comprises:

a sense circuit coupled to the common mode feedback amplifier; and

a pull-up circuit coupled to the plurality of input transistors.

9. The fully differential amplifier of claim 8, further comprising a common mode feedback network coupled to the sense circuit, the common mode feedback amplifier and the plurality of input transistors.

10. The fully differential amplifier of claim 8, wherein the sense circuit comprises:

a first transistor having a gate coupled to receive a common mode input signal from the common mode feedback network, the first transistor having a drain coupled to the pull-up circuit; and

a second transistor having a drain coupled to the drain of the first transistor.

11. The fully differential amplifier of claim 10, wherein the common mode feedback network comprises:

a first resistor coupled in parallel with a first capacitor to form a first resistor-capacitor network, the first resistor-capacitor network coupled between a first one of the outputs of the fully differential amplifier; and the gate of the first transistor of the sense circuit; and

a second resistor coupled in parallel with a second capacitor to form a second resistor-capacitor network, the second resistor-capacitor network coupled to the first resistor-capacitor network, the second resistor-capacitor network coupled between a second one of the outputs of the fully differential amplifier; and the gate of the first transistor of the sense circuit.

12. The fully differential amplifier of claim 8, further comprising an output stage having a plurality of output transistors coupled to receive a supply voltage, wherein the plurality of input transistors is coupled to receive the supply voltage.

13. The fully differential amplifier of claim 10, further comprising an output stage having a plurality of output transistors coupled to receive a supply voltage, wherein the plurality of input transistors is coupled to receive the supply voltage.

14. The fully differential amplifier of claim 7, wherein the fully differential amplifier is implemented with CMOS technology.

15. The fully differential amplifier of claim 10, wherein the common mode feedback network comprises a switching capacitor network.

16. A system, comprising:

a dipole antenna; and

an amplifier circuit operatively coupled to the dipole antenna, the amplifier circuit comprising:

a first stage comprising a common mode feedback amplifier;

a second stage comprising a plurality of input transistors; and

a start-up circuit coupled between the first and second stages.

17. The system of claim 16, wherein the start-up circuit comprises:

a sense circuit coupled to the common mode feedback amplifier; and

a pull-up circuit coupled to the plurality of input transistors.

18. The system of claim 17, wherein the sense circuit comprises:

a first transistor having a gate coupled to receive a common mode input signal from the common mode feedback network, the first transistor having a source coupled to the pull-up circuit; and

a second transistor having a drain coupled to the source of the first transistor.

19. The system of claim 18, wherein the amplifier circuit is an automatic gain control amplifier.

20. The system of claim 18, wherein the amplifier circuit is a filter.

21. The system of claim 18, wherein the amplifier circuit is a multiplexer.

22. A system, comprising:

a digital signal processor; and

an amplifier circuit operatively coupled to the digital signal processor, the amplifier circuit comprising:

a first stage comprising a common mode feedback amplifier;

a second stage comprising a plurality of input transistors; and

a start-up circuit coupled between the first and second stages.

23. The system of claim 22, wherein the start-up circuit comprises:

a sense circuit coupled to the common mode feedback amplifier; and

a pull-up circuit coupled to the plurality of input transistors.

24. The system of claim 23, wherein the wherein the sense circuit comprises:

a first transistor having a gate coupled to receive a common mode input signal from the common mode feedback network, the first transistor having a source coupled to the pull-up circuit; and

a second transistor having a drain coupled to the source of the first transistor.

25. The system of claim 24, wherein the amplifier circuit is part of an analog to digital converter.

26. The system of claim 25, wherein the amplifier circuit is part of a digital to analog converter.

27. A fully differential amplifier, comprising:

means for sensing a saturation of a common mode feedback in the fully differential amplifier; and

means for returning the fully differential amplifier to a normal mode of operation based on the sensing of the saturation of the common mode feedback.

28. The fully differential amplifier of claim 27, wherein the means for sensing comprises means for receiving a common mode feedback signal at an input of a sense circuit, and wherein the fully differential amplifier further comprises a plurality of input transistors coupled to receive a supply voltage and an output stage having a plurality of output transistors coupled to receive the supply voltage.

29. The fully differential amplifier of claim 28, further comprising means for generating the common mode feedback signal.